A METHOD AND STRUCTURE FOR LAYOUT OF CELL CONTACT AREA FOR SEMICONDUCTOR INTEGRATED CIRCUITS

ABSTRACT OF THE DISCLOSURE

An EEPROM integrated circuit structure. The structure has a substrate that includes a surface region. Preferably, the surface region is provided within a first cell region. The structure also has a gate dielectric layer of first thickness overlying the surface of the substrate region and a select gate overlying a first portion of the gate dielectric layer. A floating gate is overlying a second portion of the gate dielectric layer and is coupled to the select gate. An insulating layer is overlying the floating gate. A control gate is overlying the insulating layer and is coupled to the floating gate. A tunnel window provided in a stripe configuration is formed within a portion of the gate dielectric layer. The portion of the gate dielectric layer is characterized by a second thickness, which is less than the first thickness.